REMARKS

Claims 1 to 26 are pending in the above-identified application when last examined. Applicant has added claims 27 and 28.

§ 103 Rejections

The Examiner rejected claims 1 to 26 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,260,079 ("White") in view of U.S. Patent No. 4,220,876 ("Ray"). Addressing Applicant's arguments, the Examiner stated:

> 8. In the remarks, applicants argued in substance that Ray does not teach or suggest that circuit 44 does not decouple instrument 10 from either bus 50 either physically or electrically. But Ray teaches a circuit that renders devices connected thereto non-conductive and thereby electrically isolates hem from the bus [Abstract]. Specifically, Ray teaches that circuit 44 is interposed between a bus input terminal 46 and an external bus 50 [col. 3, lines 5-11].
>
> 9. Furthermore, Ray teaches the operation of the circuit [col. 4, lines 1-40], and as Applicant agrees, operation of the circuit when the voltage output from a voltage circuit falls below a predetermined threshold [col. 4, lines 13-40]. With particular regard to the decoupling of the bus, Ray teaches that when the voltage output falls below said threshold, node 48 presents a high impedance to the bus 50 [col. 4, lines 34-40], preventing circuit 44 from loading the bus. Because node 48 is presents a high impedance, no electrical current may pass from bus input terminal 46, or circuits connected thereto, to bus 50, thereby electrically decoupling and isolating any such circuits from bus 50, substantially as claimed.
>
> 10. Ray discloses the process by which node 48 presents a high impedance [col. 4, lines 13-40], wherein the voltage threshold is detected by diodes 68, 70, and 72, which in turn control transistor switch 64. In summary, when the voltage falls below the threshold, current is prevented from flowing through segments 52-62, comprising node 48, thereby electrically decoupling and isolating circuits coupled to node 48 from bus 50. This is not only electrically decouples resistors 58 and 60, as admitted by Applicant, but also any other circuits coupled to node 48, such as those coupled to bus input terminal 46. The effect of current flow in the circuit when transistor switch 64 is rendered non-conductive, as is well known to one of ordinary skill in the art.

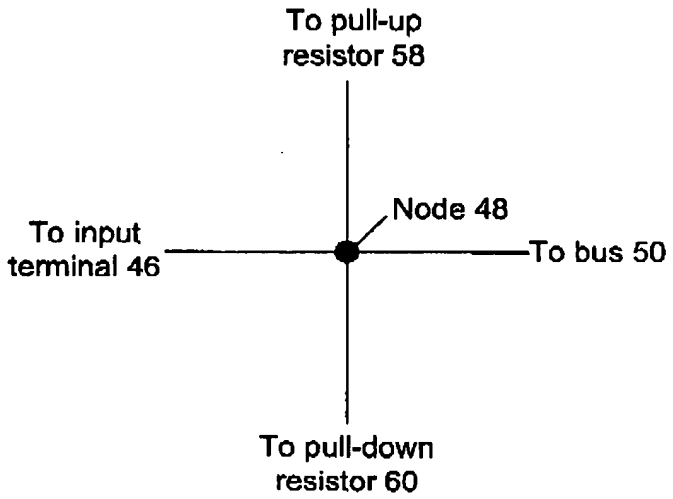
March 9, 2005 Final Office Action, pp. 4 and 5 (emphasis added). Applicant respectfully traverses.

In paragraph 8, the Examiner asserted that bus termination circuit 44 is interposed between input terminal 46 of a device and bus 50. March 9, 2005 Final Office Action, p. 4. However, Fig. 2

clearly shows that termination circuit 44, input terminal 46, and bus 50 are all connected at node 48. Thus, bus termination circuit 44 is not interposed between input terminal 46 and bus 50.

In paragraph 9, the Examiner asserted that bus termination circuit 44 causes node 48 to present high impedance to bus 50. March 9, 2005 Final Office Action, p. 5. The Examiner was referring to Ray where it states that "[s]ince no current flows through either resistor 58 or 60, then node 48 presents a high impedance to bus 50." Ray, col. 4, lines 34 and 35. However, this statement must be taken in the context that the line driver and receiver of the device at input terminal 46 also present high impedance on node 48 when both the device and bus termination circuit 44 are turned off. This does not detract from the fact that it is physically impossible for bus termination circuit 44 to disconnect input terminal 46 from bus 50 at node 48.

In paragraph 10, the Examiner asserted that by preventing current from following through elements 52 to 62, bus termination circuit 44 creates high impedance at node 48. March 9, 2005 Final Office Action, p. 5. Unfortunately, the Examiner misunderstood how bus termination circuit 44 works. Below is a simplified figure that may help the Examiner understand the connection between the three relevant elements: bus termination circuit 44, input terminal 46, and bus 50.



The Examiner appeared to agree with the Applicant that current cannot flow through resistors 58 and 60 when supply voltage Vcc falls below a threshold. This means that the north and south paths from node 48 are blocked when supply voltage Vcc falls below a threshold. However, this does not mean that node 48 is blocked. Instead, the east and west paths between input terminal 46 and bus 50 through node 48 remain open.

Again, the Examiner may be confused by the language of Ray as discuss above. The language in Ray describes when the line driver and receiver at input terminal 46 also have high impedance, thereby blocking the west path from node 48. However, it is still physically impossible for bus termination circuit 44 to disconnect input terminal 46 from bus 50 at node 48. To further support this argument, Applicant has submitted a Rule 312 Declaration from the system architect Michel Ceklcov at 3PARdata, Inc. Accordingly, claim 1 is patentable over the combination of Ray and White.

Claims 2 to 13 depend from claim 1 and are patentable over the cited references for at least the same reasons as claim 1.

Independent claim 14 recites similar limitations as claim 1, and therefore is patentable over the cited references for at least the same reasons as claim 1. Claims 15 to 26 depend from claim 14 and are patentable over the cited references for at least the same reasons as claim 14.

New Claims

Applicant has added a claim 27 that depends from claim 1. Claim 27 recites that the coupled buses are I2C buses. Claim 27 is patentable over the combination of White and Ray because White discloses only SCSI buses and Ray discloses bus termination circuits. Furthermore, I2C bus is an open drain bus where the lines are pulled to supply voltage Vcc when they are quiescent. Thus, the I2C bus does not require bus termination circuits.

Applicant has added a claim 28 that depends from claim 14. Claim 28 recites similar limitations as claim 27 and is patentable over the cited references for at least the same reasons as claim 27.

In summary, claims 1 to 26 were pending in the above-identified application when last examined. Applicant has added claims 27 and 28. For the above reasons, Applicant respectfully requests the Examiner with withdraw the claim rejections and allow claims 1 to 28. Should the Examiner have any questions, please call the undersigned at (408) 382-0480x206.

Certification of Facsimile Transmission

I hereby certify that this paper is being facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature 6/9/2005 Date

Respectfully submitted,

David C. Hsia
Attorney for Applicant(s)
Reg. No. 46,235